EN-QDD800-SR8

800Gb/s QSFP-DD SR8 Transceiver module

The 800G QSFP-DD SR8 Transceiver is designed to transmit and receive serial optical data links up to 106.25 Gb/s data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with the high-performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 800G Ethernet specs and QSFP-DD MSA.

Features

- Up to 106.25 Gbps data rate per channel by PAM4 modulation on media side
- Up to 106.25 Gbps data rate per channel by PAM4 modulation on host side
- MPO-16 APC optical interface
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Maximum link length of 50M on OM4 MMF
- Power dissipation: <16W
- International class 1 laser safety certified
- Operating temperature range: 25℃ ~ +70℃
- Compliant with ROHS2.0

Applications

- 800GBASE Ethernet
- Switch & Router Connections
- Data Centers
- Other 800G Interconnect Requirements.

Standards

- IEEE 802.3db™-2022
- IEEE 802.3ck™-2022
- QSFP-DD HW Rev 6.2
- CMIS Rev 4.0 or later version

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		53.125±50ppm		
Modulation format				PAM4		
Center wavelength		nm	840		870	
RMS Spectral Width	RMS	nm			0.65	
Average Launch Power per Lane	TXPx	dBm	-4.6		4	
Outer Optical Modulation Amplitude (OMAouter), each lane (min) for max (TECQ, TDECQ)≤1.8 dB	OMAouter	dBm	–2.6		3.5	
for 1.8<max (TECQ, TDECQ)≤4.4 dB			-4.4+max (TECQ, TDECQ)			
Transmitter excursion, each lane	DPx	dB			2.3	
Optical Extinction Ratio	ER	dB	2.5			
Transmitter and dispersion penalty eye closure for PAM4,each lane	TDECQ	dB			4.4	
Transmitter transition time	Tr、 Tf	ps			17	
$RIN_{14}OMA$		dB/Hz			-132	
Encircled Flux	FLX	dBm	≥86% at 19um			
			<30%at 4.5um			
Optical Return Loss Tolerance	ORL	dB			14	
Average launch power of OFF Transmitter, each lane		dBm			-30	
Receiver (per Lane)						
Signaling Speed per Lane		GBd		53.125± 50ppm		
Modulation format				PAM4		
Center wavelength		nm	840		870	
Damage Threshold	DT	dBm	5			
Average receive Power per Lane	RXPx	dBm	-6.3		4	
Receive power, each lane (OMAouter)		dBm			3.5	
Receiver reflectance	Rfl	dB			-15	
Receiver sensitivity (OMAouter)		dBm				

for TECQ ≤ 1.8 dB for 1.8 < TECQ ≤ 4.4 dB					-4.4 -6.2+TECQ	
Stressed receiver sensitivity(OMAouter),each lane	S	dBm			-1.8	BER=2.4E-4
Los Assert	LOS_A	dBm		-11		
Los De-assert	LOS_D	dBm		-10		

Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
EN-QDD800-SR8	QSFP-DD	800G	VCSEL	-4.6~4dBm	PD	< -4.4dBm@ 2.4E-4	25~70°C	50m	RoHS	800G Base SR8

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	25	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Media side Bit Rate (Per channel)	BR	Gbps		106.25	
Host side Bit Rate (Per channel)	BR	Gbps		106.25	

Optical Interface

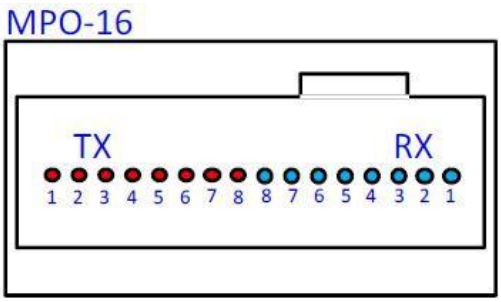

Figure 1: Optical lane sequence

Note：Optical interface is 8° APC MPO-16.Lane sequence is shown in figure 1.

Principal diagram

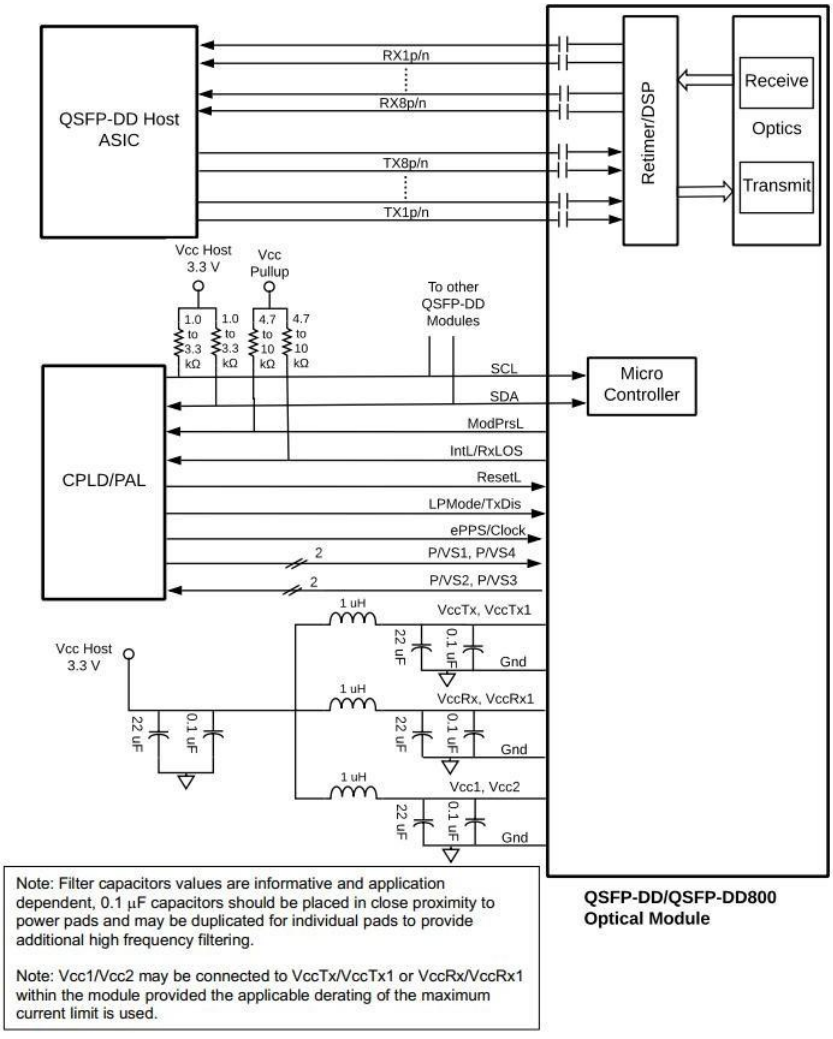

Figure 2: Module Principal Diagram

Electric Ports Definition

Parameter	Min	Typ	Max	Unit	Notes
Supply voltage	3.135		3.465	V	
Signaling rate, each lane	53.125 -50ppm	53.125	53.125 +50ppm	GBd	
Module input characteristics					
Differential peak-to-peak input voltage tolerance	750			mV	TP1a
Peak-to-peak AC common-mode voltage tolerance					TP1a
Low-frequency, VCM_{LF}	32			mV	
Full-band, VCM_{FB}	80			mV	
Differential-mode to common-mode return loss, RLcd	See IEEE Std 802.3ck™-2022 Equation(120G-2)			dB	TP1
Effective return loss, ERL	8.5			dB	TP1
Differential termination mismatch			10	%	TP1
Module stressed input tolerance	See IEEE Std 802.3ck™-2022 120G.3.4.3				TP1a
Single-ended voltage tolerance	-0.4		3.3	V	TP1a
DC common-mode voltage tolerance	-0.35		2.85	V	TP1
Module output characteristics					
Peak-to-peak AC common-mode voltage					TP4
Low-frequency, VCM_{LF}			32	mV	
Full-band, VCM_{FB}			80	mV	
Differential peak-to-peak output voltage					TP4
Short mode			600	mV	
Long mode			845	mV	
Eye height	15			mV	TP4
Vertical eye closure, VEC			12	dB	TP4
Common-mode to differential-mode return loss, RLdc	See IEEE Std 802.3ck™-2022 Equation(120G-1)			dB	TP4
Effective return loss, ERL	8.5			dB	TP4
Differential termination mismatch			10	%	TP4

Parameter	Min	Typ	Max	Unit	Notes
Transition time	8.5			ps	TP4
DC common-mode voltage tolerance	-0.35		2.85	V	TP4
IIC communication					
IIC Clock frequency	100		1000	kHz	
Clock stretching			500	μs	
Data In Hold Time	0			μs	
Data In Setup Time	0.1			μs	

Pin Description

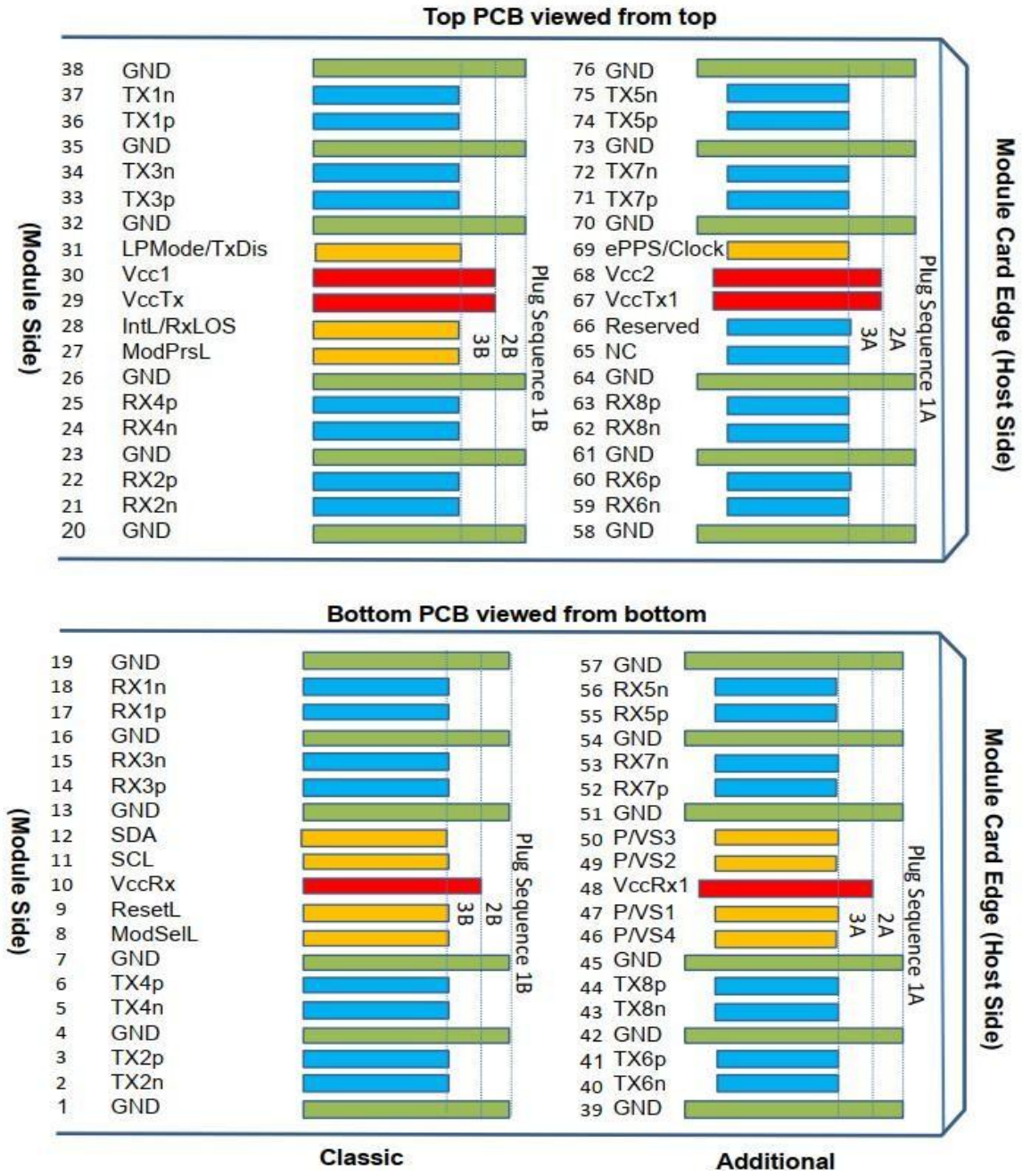

Figure 3: Electrical Pin-out Details

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	TWI Serial Interface Clock	
12	LVCOMS-I/O	SDA	TWI Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	ModPrsL	Module Present	
28	LVTTL-0	IntL/RxLOS	Interrupt/optional RxLOS	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	
32		GND	Ground	1

PIN	Logic	Symbol	DESCRIPTION	NOTE
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data output	
45		GND	Ground	1
46	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4	5
47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1	5
48		VccRx1	+3.3V Power Supply	2
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2	5
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3	5
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1

PIN	Logic	Symbol	DESCRIPTION	NOTE
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx 1	+3.3 V Power Supply	2
68		Vcc2	+3.3 V Power Supply	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	6
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data output	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data output	
76		GND	Ground	1

Notes:

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a state current of 1500 mA.

Note 3: Reserved and no Connect pads recommended to be terminated with 10kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A,1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFPDD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.

Note 6: ePPS/Clock if not used recommended to be terminated with 50Ω to ground on the host.

Module Memory Map

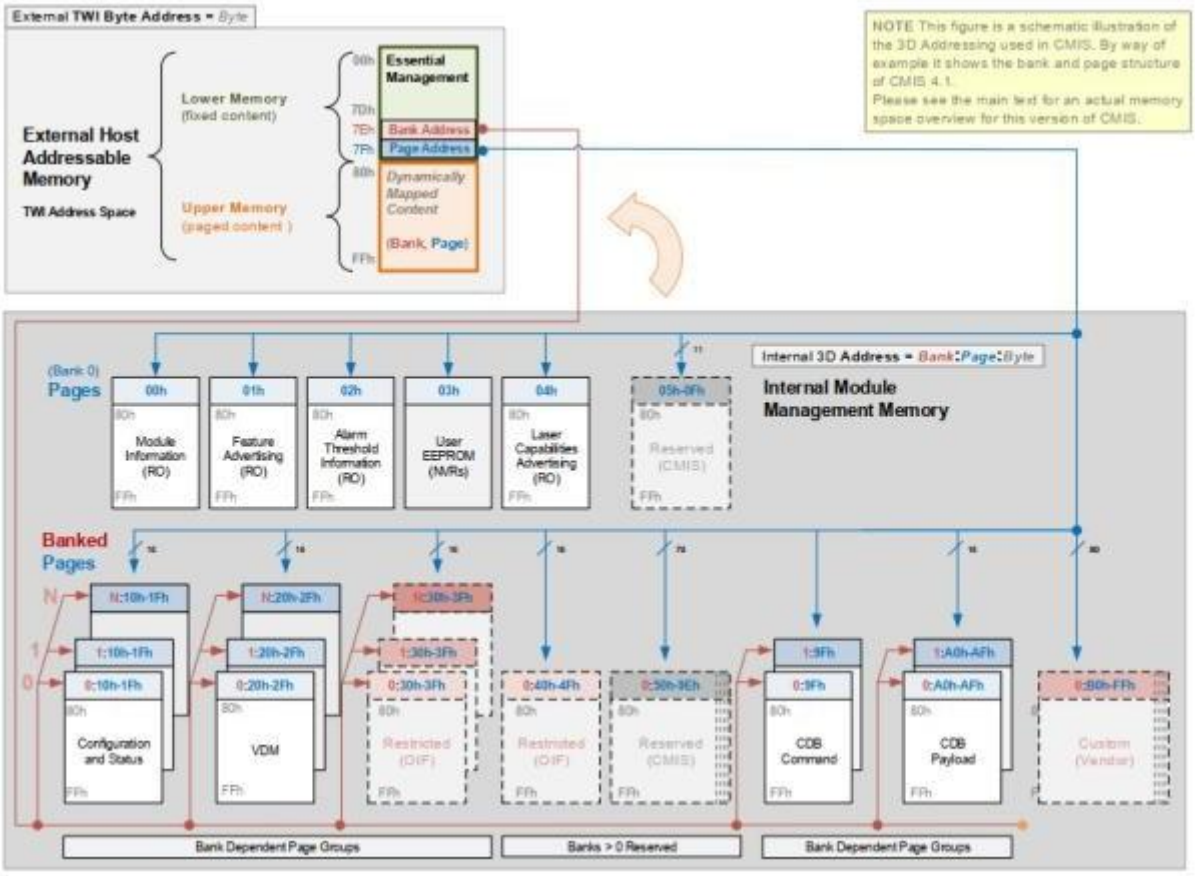

Figure 4: Digital Diagnostic Memory Map

Host Board Power Supply Filtering

Any voltage drops across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, to minimize the voltage drop and the amount of noise coupled to the module. Hosts supporting higher power classes modules may require additional design considerations, in order to minimize the voltage, drop and the amount of noise coupled to the module.

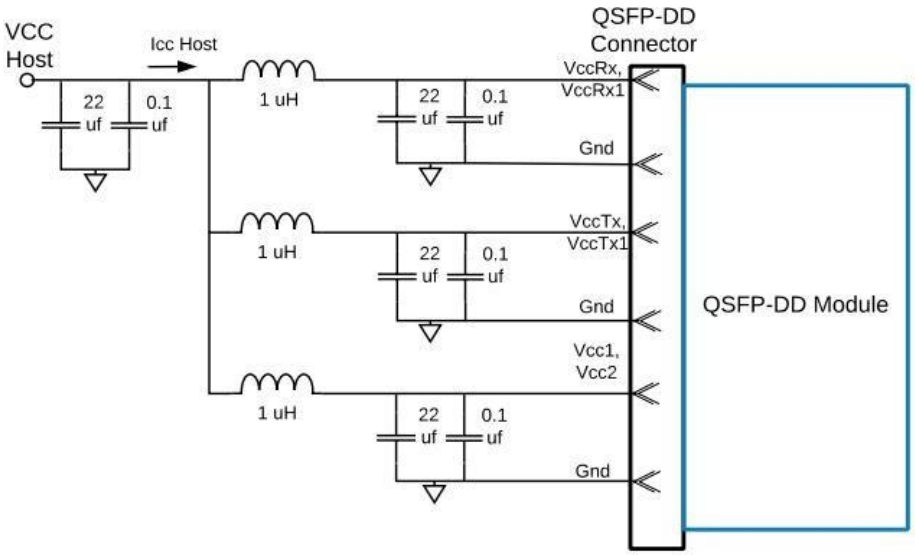

Figure 5: Recommended Host Board Power Supply Filtering