EN-QDD800DAC-xM
800G to 800G QSFP-DD Passive DAC TWINAX Cable

Features and Benefits

- Compatible with IEEE 802.3ck
- Supports aggregate data rates of 800Gbps(PAM4)
- Optimized construction to minimize insertion loss and crosstalk
- Pull-to-release slide latch design
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customized EEPROM mapping for cable signature
- 26AWG and 28AWG cable
- 3.3V Power supply
- Temperature Range: 0~ 70 °C
- RoHS Compliant

Product Applications

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Test and measurement equipment

Industry Standards

- 800G Ethernet (IEEE 802.3ck)
- InfiniBand NDR

General Description

The 800G QSFP-DD DAC is a high-speed, cost-effective alternative to fiber optics in 800G Ethernet applications. It contains 16 high-speed copper pairs, each operating at data rates of up to 100Gb/s.

This cable is compliant with IEEE 802.3ck Ethernet standard and QSFP-DD MSA Compliant (Multi-Source Agreement). With these features, they provide power-efficient connectivity for short-distance interconnects and enable higher port bandwidth, density and configurability in the data centers.

Pin Descriptions

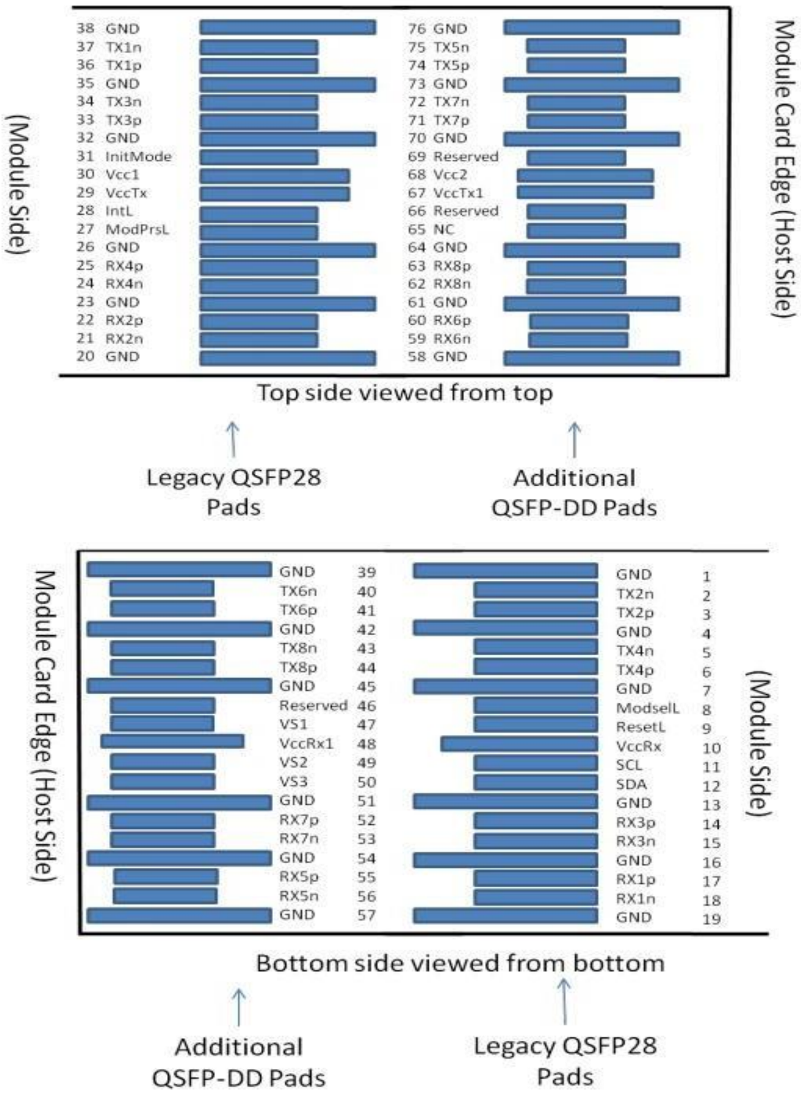
QSFP-DD Pin Function Definition

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS- I/O	SCL	2-wire serial interface clock
12	LVCMOS- I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output

19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		Vcc Tx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power Mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46		Reserved	

47		VS1	
48		VccRx1	+3.3V Power supply
49		VS2	
50		VS3	
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	
66		Reserved	
67		VccTx1	+3.3V Power supply
68		VCC2	+3.3V Power supply
69		Reserved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input

75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground



General Product Characteristics

QSFP-DD DAC Specifications	
Number of Lanes	Tx8 Rx8
Channel Data Rate	106. 25Gbps
Operating Temperature	0 to + 70°C
Storage Temperature	-40 to + 85°C
Supply Voltage	3.3 V nominal
Electrical Interface	76pins edge connector
Management Interface	Serial, I^2C

High Speed Characteristics

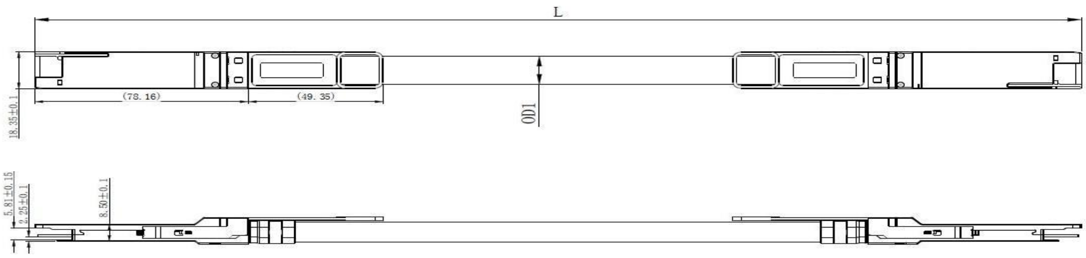
Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-19.75			dB	At 26.56 GHz
Differential Return Loss	SDD11 SDD22			See 1	dB	At 0.05 to 26.56GHz
				See 2	dB	At 26.56 to 40 GHz
Common-mode to common-mode output return loss	SCC11 SCC22			-2	dB	At 0.2 to 40GHz
Differential to common Mode Conversion Loss	SCD21-SDD21			-10	dB	At 0.05 to 12.89 GHz
				See3		At 12.89 to 40 GHz

Notes:

1. Reflection Coefficient given by equation SDD11(dB) <22-10(f/26.56), with f in GHz
2. Reflection Coefficient given by equation SDD11(dB) <15-3(f/26.5), with f in GHz
3. Reflection Coefficient given by equation SCD21-CDD21(dB) < 14-0.3108*f, with f in GHz

Mechanical Specifications

The connector is compatible with the QSFP-DD specification.



Length (m)	Cable AWG
1	28
1.5	28
2	26

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1(>2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B	Compliant with Standards
	CENELEC EN55022 Class B	
	CISPR22 ITE Class B	
RF Immunity(RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives （EU） 2015/863	RoHS （EU）2015/863 compliant
REACH Compliance	REACH Regulation (EC) No 1907/2006	REACH (EC) No 1907/2006 compliant