PRODUCT SPECIFICATION

Product Name : EN-OSFP800-DR8-M16

INDEX

1 DESCRIPTION

1.1 Product Function

The 800G OSFP DR8 Transceiver is designed to transmit and receive serial optical data links up to 106.25 Gbps data rate (per channel) by PAM4 modulation format over single-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with high performance Sipho modulator. It is compliant with 800G Ethernet specs and OSFP MSA.

1.2 Product Application

800GBASE-DR8 Ethernet

Switch & Router Connections

Data Centers

Other 800G Interconnect Requirements.

1.3 Standards

IEEE 802.3bs

CMIS Rev 5.2 or later version

OSFP MSA

2 SPECIFICATION

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Notes
Transmit characteristics					
Signaling rate		53.125 ±100ppm		GBd	
Modulation format		PAM4			
Wavelength	1304.5	1311	1317.5	nm	

Parameter	Min	Typ	Max	Unit	Notes
Side-mode suppression ratio(SMSR)	30			dB	
Average launch power	-2.9		4	dBm	
Outer Optical Modulation Amplitude(OMA_{outer})	-0.8		4.2	dBm	
Launch power in OMA_{outer} minus TDECQ	-2.2			dBm	
Transmitter and dispersion eye closure for PAM4(TDECQ)			3.4	dB	
Extinction ratio	3.5			dB	
Average launch power of OFF transmitter			-15	dBm	
$RIN_{21.4}OMA$			-136	dB/Hz	
Optical return loss tolerance			21.4	dB	
Transmitter reflectance			-26	dB	
Receive characteristics					
Signaling rate		53.125 ±100ppm		GBd	
Modulation format		PAM4			
Wavelength	1304.5		1317.5	nm	
Damage threshold		5		dBm	
Average receive power	-5.9		4	dBm	
Receive power (OMA_{outer})			4.2	dBm	
Receiver reflectance			-26	dB	
Receiver sensitivity (OMA_{outer})			-3.9	dBm	
Stressed receiver sensitivity (OMA_{outer})			-1.9	dBm	
Conditions of stressed receiver sensitivity test:					
Stressed eye closure for PAM4 (SECQ)		3.4		dB	
SECQ – 10log10(C_{eq})			3.4	dBm	

3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

4 OPTIC PORTS DEFINITION

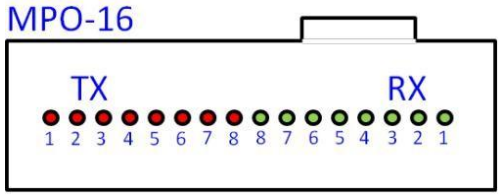

Figure 1. Optical lane sequence

Note：Optical interface is 8° APC

PRINCIPLE DIAGRAM

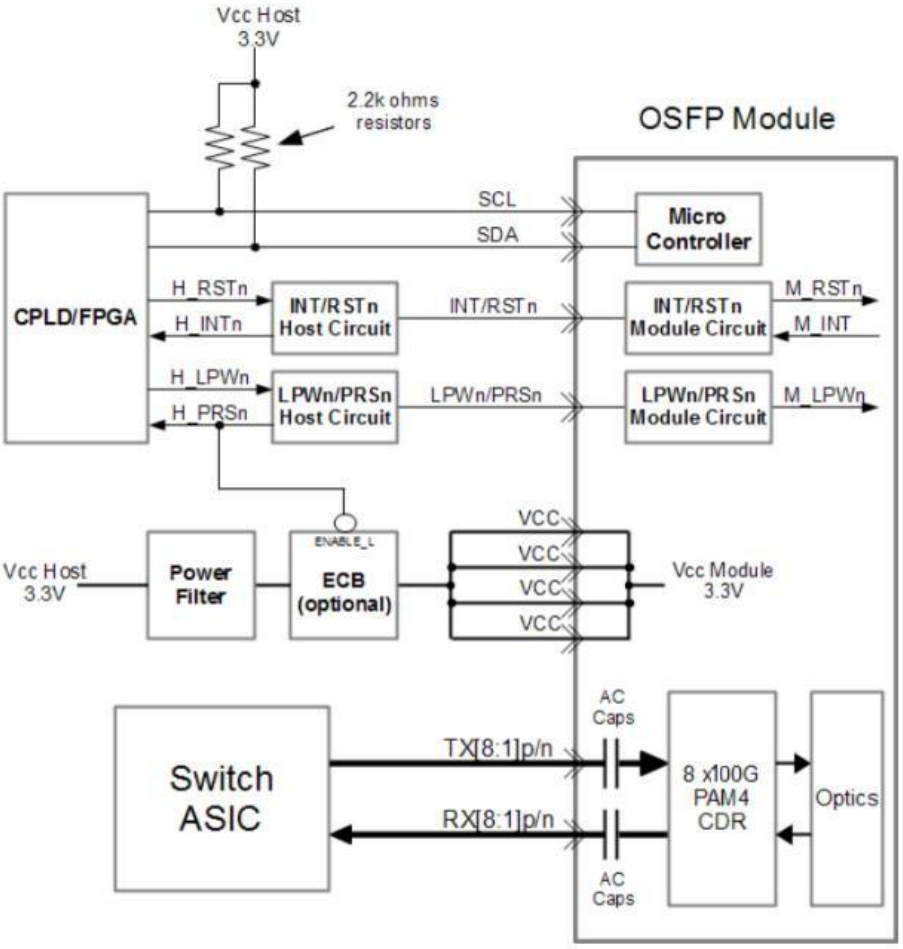

Figure 2. Module Principle Diagram

5 ELECTRIC PORTS DEFINITION

Parameter	Min	Typ	Max	Unit	Notes
Supply voltage	3.135		3.465	V	
Signaling rate, each lane		53.125 ±100ppm		GBd	
Module input characteristics					
Differential peak-to-peak input voltage tolerance	750			mV	TP1a
AC common-mode RMS voltage tolerance	25			mV	TP1a
Differential termination mismatch			10	%	TP1
Module stressed input tolerance	See IEEE P802.3ck™/D3.0 120G.3.4.3				TP1a

Parameter	Min	Typ	Max	Unit	Notes
Single-ended voltage tolerance	-0.4		3.3	V	TP1a
DC common-mode voltage tolerance	-0.35		2.85	V	TP1
Module output characteristics					
AC common-mode output voltage(RMS)			25	mV	TP4
Differential peak-to-peak output voltage					TP4
Short mode			600	mV	
Long mode			845	mV	
Eye height	15			mV	TP4
Vertical eye closure, VEC			12	dB	TP4
Differential termination mismatch			10	%	TP4
Transition time	8.5			ps	TP4
DC common-mode voltage tolerance	-0.35		2.85	V	TP4
IIC communication					
IIC Clock frequency	100		1000	kHz	
Clock stretching			500	us	
Data In Hold Time	0			us	
Data In Setup Time	0.1			us	

6 Pin Description

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	
2	CML-I	Tx2p	Transmitter Data Non-Inverted	
3	CML-I	Tx2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	Tx4p	Transmitter Data Non-Inverted	

PIN	Logic	Symbol	DESCRIPTION	NOTE
6	CML-I	Tx4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	Tx6p	Transmitter Data Non-Inverted	
9	CML-I	Tx6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	Tx8p	Transmitter Data Non-Inverted	
12	CML-I	Tx8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Open-Drain with pull up resistor on Host
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	See pin description
18		GND	Ground	
19	CML-O	Rx7n	Receiver Data Inverted	
20	CML-O	Rx7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	Rx5n	Receiver Data Inverted	
23	CML-O	Rx5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	Rx3n	Receiver Data Inverted	
26	CML-O	Rx3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	Rx1n	Receiver Data Inverted	
29	CML-O	Rx1p	Receiver Data Non-Inverted	

PIN	Logic	Symbol	DESCRIPTION	NOTE
30		GND	Ground	
31		GND	Ground	
32	CML-O	Rx2p	Receiver Data Non-Inverted	
33	CML-O	Rx2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	Rx4p	Receiver Data Non-Inverted	
36	CML-O	Rx4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	Rx6p	Receiver Data Non-Inverted	
39	CML-O	Rx6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	Rx8p	Receiver Data Non-Inverted	
42	CML-O	Rx8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	See pin description
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	Open-Drain with pull up resistor on Host
48		GND	Ground	
49	CML-I	Tx7n	Transmitter Data Inverted	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	Tx5n	Transmitter Data Inverted	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	

PIN	Logic	Symbol	DESCRIPTION	NOTE
54		GND	Ground	
55	CML-I	Tx3n	Transmitter Data Inverted	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	Tx1n	Transmitter Data Inverted	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	
60		GND	Ground	

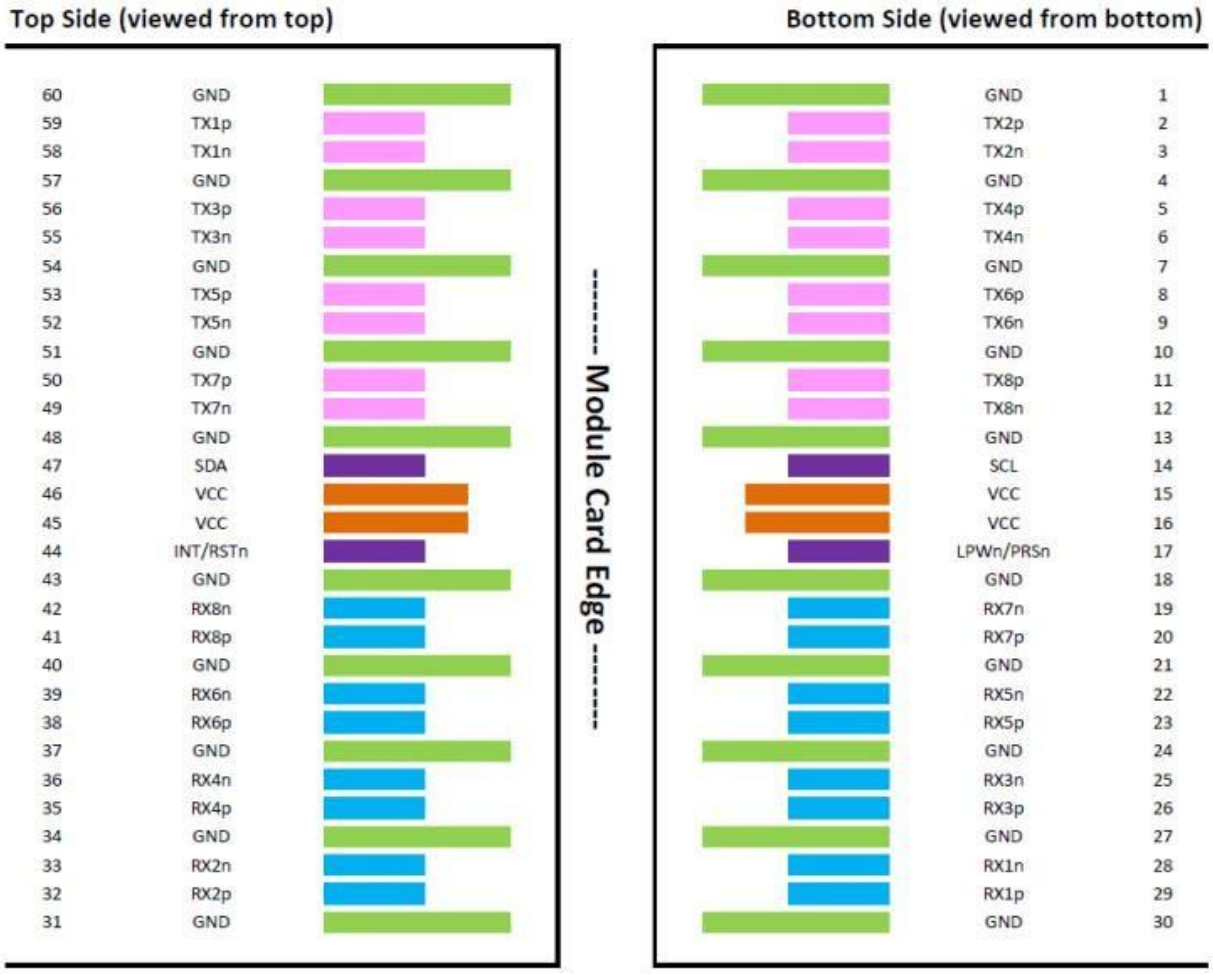

Figure 3. Electrical Pin-out Details

7 Module Memory Map

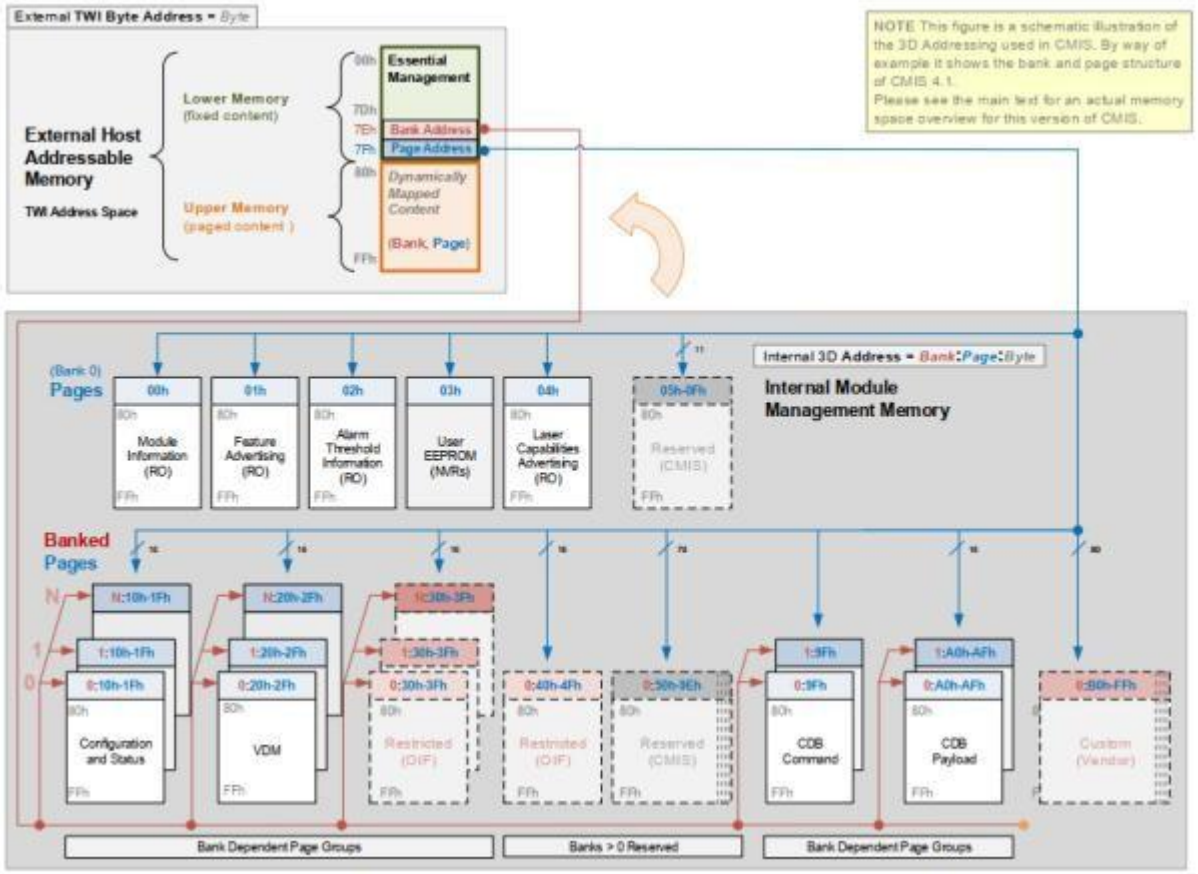

Figure 4 Digital Diagnostic Memory Map

8 Host Board Power Supply Filtering

Figure 5 provides an example implementation for a 3.3V power filter on the host board.

If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

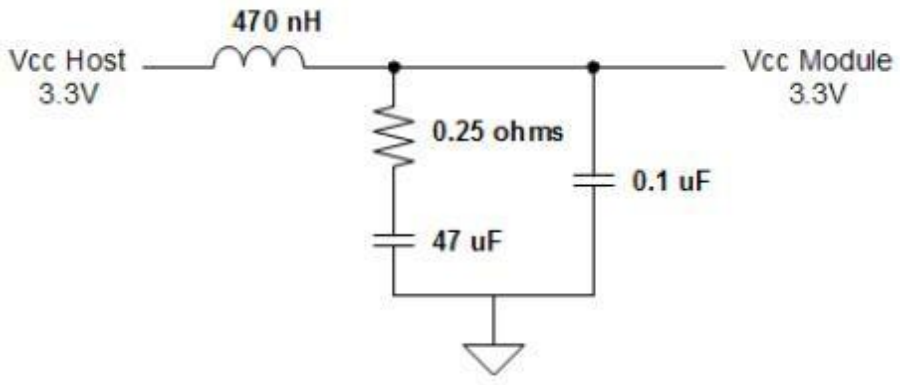

Figure 5 Recommended Host Board Power Supply Filtering

9 Package Outline

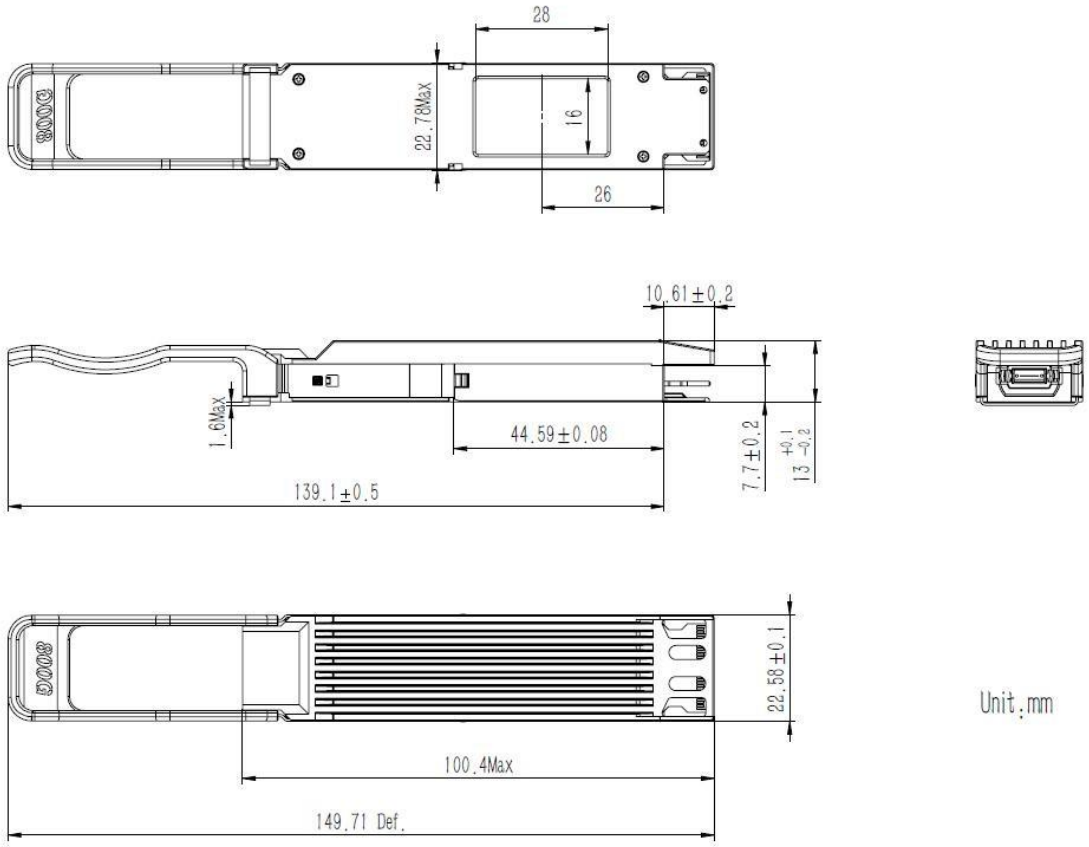

Figure 6 Package Outline