400G QSFP-DD ZR+ Pro Transceiver EN-QDD-DCO-ZR+P

400G QSFP-DD ZR+ Pro Transceiver EN-QDD-DCO-ZR+P

Features

- Compliant with QSFP-DD MSA, Type 2B package
- Compliant with Open ZR+ MSA and OIF 400ZR MSA, support OFEC and CFEC FEC
- Line rate 100G/200G/300G/400G
- Client rate 1/2/3/4x100GbE or 1x400GbE
- C-band tunable, supports 100/75/50GHz grid spacing, support 0.1GHz fine tuning.
- EDFA inside, High output Power, max TX power +4dBm at 193.7THz, +1dBm at C-band
- TX VOA inside, output power -10~1dBm tunable
- Support ingress LF hold-off time configure.
- Support hitless firmware upgrade.
- Compact size (18.4 mm x 93.4 mm x 8.5 mm)
- Duplex LC connector
- Operating case temperature: 0℃ to 70°C
- Single 3.3 V power supply
- Maximum power consumption 22.5W (400GbE)
- RoHS 2 compliant

Applications

- Edge DCI with extended Reach or with OLP protection
- IP Over Metro or Long Haul DWDM
- Up to 80Km unamplified 400G P2P link

Compliance

- Open ZR+ MSA 2.0 and OIF-400ZR-02.0
- OIF-CMIS-05.2

Description

The E.C.I. NETWORKS's **EN-QDD-DCO-ZR+P 400G ZR+ PRO** Transceiver is a high performance, high output power, cost effective module for optical data communication applications from 100G to 400G. The **EN-QDD-DCO-ZR+ PRO** is designed to 100G/200G long haul and 300G/400G Metro IP over DWDM applications without inline chromatic dispersion compensation.

The **EN-QDD-DCO-ZR+ PRO** is a C-Band optical frequency tunable coherent optical module, combines 7nm coherent DSP ASIC functionality with best-in-class ultra-narrow line-width tunable lasers, high speed modulators and high responsively coherent receivers to deliver highperformance at 200G DP-QPSK / 300G DP-8QAM / 400G DP-16QAM modulation format at 60G baud rate and 100G DP-QPSK at 30G baud rate. With EDFA and VOA inside the TX optical path the output optical power is -10~1dBm tunable, at the 400G 80Km Gray mode (193.7THz) the output power is 4dBm.

The **EN-QDD-DCO-ZR+ PRO** coherent transceiver Compliant withthe OIF QSFP-DD MSA. Digital diagnostics functions are available via an I2C interface as specified by the QSFP-DDMSA. Mechanical dimensions, connectors and footprint conform to QSFP-DD MSA. The module is 18.4 mm x 93.4 mm x 8.5 mm in size and hot pluggable by 76 PIN PAD andhost connector. The maximum power consumption is 22.5W(400GbE) and power supply voltage is +3.3 V

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage temperature	Ts	-40		85	℃	
Power supply	Vcc	-0.3	3.3	3.6	V	not damaged
Relative humidity	RH	5		85	%	Non-condensing
Receiver damage threshold	PRdmg	10			dBm	Total optical power
ESD Sensitivity				1000	V	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature		T_C	0		70	℃
Power supply voltage		V_{CC}	3.135	3.3	3.465	V
		I_{CC}			7.5	A
Maximum sustained peak Current(<500ms)					7.8	A
Maximum Instantaneous peak current(<50us)					9.4	A
Electro-Static discharge		ESD			1000	V
Power Consumption		P_D			22.5(400GbE)	W
					23.5(4×100GbE)	
Relative humidity		RH	15		85	%
Client Mode	400G (400ZR)		1 x 400GAUI-8			
			4 x 100GAUI-2			
	400G (400ZR+)		1 x 400GAUI-8			
			4 x 100GAUI-2			
	300G (300ZR+)		3 x 100GAUI-2			
	200G (200ZR+)		2 x 100GAUI-2			
			2 x CAUI-4			
	100G (100ZR+)		1 x 100GAUI-2			
			1 x CAUI-4			
Transmission Distance	400G (400ZR)				120	Km
	400G (400ZR+)				450	
	300G (300ZR+)				600	
	200G (200ZR+)				1000	
	100G (100ZR+)				2000	
Power Supply Noise		Vrip			1%	DC-1MHz
					2%	1-10MHz

Optical & Electrical Characteristic

Tested under recommended operating conditions, unless otherwise noted

Table3-Transmitter Operating Characteristic-Optical

Parameters		Unit	Min.	Type	Max.	Note
Modulation format	400G		ZR400-CFEC-16QAM			CFEC FEC, NCG 10.8dB
			ZR400-OFEC-16QAM			OFEC FEC, NCG 11.6dB
	300G		ZR300-OFEC-8QAM			
	200G		ZR200-OFEC-QPSK			
	100G		ZR100-OFEC-QPSK			
Baud Rate	400G	GBd	59.843750000±20ppm			400ZR,SFF-8024 Media ID 3Eh/3Fh
			60.138546798±20ppm			400ZR+,SFF-8024 Media ID 46h
	300G		60.138546798±20ppm			300ZR+,SFF-8024 Media ID 47h
	200G		60.138546798±20ppm			200ZR+,SFF-8024 Media ID 48h
	100G		30.069273399±20ppm			100ZR+, SFF-8024 Media ID 49h
Transmitter frequency range		THz	191.3		196.1	
Flexible DWDM Grid		GHz	6.25			
Frequency Fine Tuning range		GHz	-5		5	bright tuning
Frequency Fine Tuning step		GHz	0.1			
Laser frequency accuracy		GHz	-1.8		1.8	
TX spectral Upper Mask		(GHz,dB)			(30.0, 0.0) (37.0,-10.0) (39.2,-15.0) (40.4,-20.0)	Refer to OIF-400ZR-02.0 13.3.201a Refer to openzrplus_2p0 11.4.10
TX spectral Lower Mask		(GHz,dB)	(30.0,-9.0) (31.3,-20.0) (31.3,-35.0)			Refer to OIF-400ZR-02.0 13.3.201b Refer to openzrplus_2p0 11.4.10
Transmitter laser disable time		ms			100	
Transmitter wavelength switching time		s			60	
Transmitter laser enable time		s			10	
Transmit Ouput Power Adjustable Range		dBm	-10		1	The absolute accuracy is ±1dB
Transmit Ouput Power at 400G 80Km Gray mode		dBm	3	4	5	At 193.7THz
Transmit Ouput Power Adjust step		dB	0.1			

Optical power setting accuracy	dB	-1		1	Diff between setting and reporting
Output power monitor accuracy	dB	-1		1	
Power stability	dB	-0.5		0.5	At fixed wavelength, room temp
		-1		1	At fixed wavelength
Total output power with Tx disabled	dBm			-20	
Total output power during wavelength switching	dBm			-20	
Transmitter reflectance	dB			-20	Looking into the Tx
Inband (IB) OSNR	dB	38			
Lorentzian linewidth	kHz			300	Tx and LO
Relative intensity noise	dB/Hz			-140	
Mean I-Q amplitude imbalance	dB			1	
Transmitter polarization dependent power	dB			1.5	
DC I-Q offset (mean perpolarization)	dB			-26	
I-Q instantaneous offset	dB			-20	

Table4- Receiver Operating Characteristic-Optical

Parameters		Unit	Min.	Type	Max.	Note	
Modulation format	400G		ZR400-CFEC-16QAM			CFEC FEC, NCG 10.8dB	
			ZR400-OFEC-16QAM			OFEC FEC, Net Coding Gain(NCG) 11.6dB，Thretical Max PreFEC BER 2.0E-2	
	300G		ZR300-OFEC-8QAM				
	200G		ZR200-OFEC-QPSK				
	100G		ZR100-OFEC-QPSK				
Baud Rate	400G	GBd	59.843750000±20ppm			400ZR,SFF-8024 Media ID 3Eh/3Fh	
			60.138546798±20ppm			400ZR+,SFF-8024 Media ID 46h	
	300G		60.138546798±20ppm			300ZR+,SFF-8024 Media ID 47h	
	200G		60.138546798±20ppm			200ZR+,SFF-8024 Media ID 48h	
	100G		30.069273399±20ppm			100ZR+,SFF-8024 Media ID 49h	
Frequency offset between received carrier and LO		GHz	-3.6		+3.6		
Input power range	400G	dBm	-12		0	Signal power, OSNR>26dB,400ZR	
			-12		0	Signal power, OSNR>24dB,400ZR+	
			-21		0	400G 80Km Gray,OSNR>34dB	
	300G		-15		0	Signal power, OSNR>21dB,300ZR+	
	200G		-18		0	Signal power, OSNR>16dB,200ZR+	
	100G		-18		0	Signal power, OSNR>12.5dB,100ZR+	
OSNR Tolerance	400G	dB/0.1nm			26	400ZR	Measured back-to-back with short optical channel
					24	400ZR+	
	300G				21	300ZR+	
	200G				16	200ZR+	

	100G				12.5	100ZR+	
non-damaging input power		dBm			10	Total power	
Optical input power monitor accuracy		dB	-2		2	Total power	
MAX FEC Pre Ber			0.017		0.020		
Chromatic dispersion tolerance	400G	ps/nm			2,400	400ZR	Tolerance to CD with ≤ 0.5 dB penalty to OSNR sensitivity when change in SOP is ≤ 1 rad/ms
					20,000	400ZR+	
	300G				40,000	300ZR+	
	200G				50,000	200ZR+	
	100G				100,000	100ZR+	
	400G 80Km Gray				2400	400ZR 80Km	
CD monitor accuracy		ps/nm	-200		200		
DGD tolerance	400G	ps	33			400ZR	OSNR penalty<0.5dB
			66			400ZR+	
	300G		83			300ZR+	
	200G		83			200ZR+	
	100G		100			100ZR+	
DGD monitor accuracy		ps	-15		15	0~40ps for 400ZR 0~100ps for 400/300/200/100ZR+	
Peak PDL tolerance		dB			3.0	Tolerance to peak PDL with ≤ 1.3dB additionnal OSNR penalty when change in SOP is ≤1 rad/ms	
					3.5	Tolerance to peak PDL with ≤ 1.8dB additionnal OSNR penalty when change in SOP is ≤1 rad/ms	
Tolerance to change in SOP		krad/s	50			With ≤ 0.5 dB additional OSNR penalty over all PMD and PDL values	
Optical return loss		dB	20			Optical reflectance at Rx connector input.	
Optical Rx_LOS Assert Threshold	400G	dBm	-20	-18	-16		
	400G 80Km Gray		-28	-26	-24		
	300G		-23	-21	-19		
	200G		-26	-24	-22		
	100G		-26	-24	-22		
Optical Rx_LOS Hysteresis		dB	1	1.5	2.5		
Optical input power transient tolerance		dB	-2		2	Tolerance to change in input power with < 0.5 dB penalty to OSNR tolerance. The 20% to 80% rise/fall times for the input power change shall be no faster	

					than 50 μs.
Service recovery time	ms			40	

The transmitter and receiver comply with the 400GAUI-8 C2M and CEI-56G-VSR-PAM4 electrical specification, Electrical interface definitions see IEEE Std 802.3-2018 Annex 120E. The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA.

Table5-Operating Characteristic-Electrical highspeed

Parameter	Symbol	Min	Max	Unit	note
400GAUI-8 C2M and 100GAUI-2 C2M Electrical Characteristics					
Transmitter(module output)					
Signaling Rate, each lane		26.5625 ± 100 ppm		GBd	PAM-4
AC common-mode output voltage (RMS)	RMS		17.5	mV	
Differential Voltage pk-pk	Vin, pp	750	900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265		UI	
Near-end Eye height，differential		70		mV	
Far-end ESMW		0.2		UI	
Far-end Eye height，differential		30		mV	
Far-end pre-cursor ISI ratio		-4.5	2.5	%	
Differential output return loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 120E
Common to differential mode conversion return loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 120E
Differential termination mismatch		-	10	%	At 1 MHz
Transition time(20% to 80%)	Trise/Tfall	9.5		Ps	20% to 80%
DC common mode voltage	Vcm	-350	2850	mV	
Receiver (module input)					
Signaling rate per lane		26.5625 ± 100 ppm		GBd	PAM-4
Differential pk-pk input voltage tolerance	Vout, pp	900		mV	
Differential input return loss (min)		Equation (83E–5)			IEEE Std 802.3-2018 Annex 120E
Differential to common-mode input returnloss (min)		Equation (83E–6)			IEEE Std 802.3-2018 Annex 120E
Differential termination mismatch			10	%	
Module stressed input test		See 120E.3.4.1			IEEE Std 802.3-2018 Annex 120E
Single-ended voltage tolerance range (min)		-0.4	3.3	V	
DC common mode voltage(min)		-350	2850	mV	
CAUI-4 C2M Electrical Characteristics					
Transmitter(module output)					
Signaling Rate, each lane		25.78125 ± 100 ppm		GBd	NRZ

AC common-mode output voltage (RMS)	RMS		17.5	mV	
Differential Voltage pk-pk	Vin, pp	750	900	mV	
Eye width	UI	0.57			
Eye height, differentia	mV	228			
Vertical eye closure	dB	5.5			
Differential output return loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 83E
Common to differential mode conversion return loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 83E
Differential termination mismatch		-	10	%	At 1 MHz
Transition time(20% to 80%)	Trise/Tfall	12		Ps	20% to 80%
DC common mode voltage	Vcm	-350	2850	mV	
Receiver (module input)					
Signaling rate per lane		25.78125 ± 100 ppm		GBd	NRZ
Differential pk-pk input voltage tolerance	Vout, pp	900		mV	
Differential input return loss (min)		Equation (83E–5)			IEEE Std 802.3-2018 Annex 83E
Differential to common-mode input returnloss (min)		Equation (83E–6)			IEEE Std 802.3-2018 Annex 83E
Differential termination mismatch			10	%	IEEE Std 802.3-2018 Annex 83E
Module stressed input test		See 83E.3.4.1			
Single-ended voltage tolerance range (min)		-0.4	3.3	V	
DC common mode voltage(min)		-350	2850	mV	

Table6-Operating Characteristic-Electrical Lowspeed

Parameters	Symbol	Unit	Min.	Max.	Note
SCL and SDA	VOL	0	0.4	V	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 45 (QSFP-DD-Hardware-rev5p0)
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 45 (QSFP-DD-Hardware-rev5p0)
InitMode, ResetL and	VIL	-0.3	0.8	V	

ModSelL IntL	VIH	2	VCC+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

Table7-Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temp
TX power monitor absolute error	DMI_TX	-1/-1.5	1/1.5	dB	-15 ~ -9 dBm ±1dB@(25~60)℃ ±1dB@(0~70)℃
RX power monitor absolute error	DMI_RX	-1.5/-2	1.5/2	dB	±1.5dB @ (-12 ~ 0) dBm ±2dB @ (-18 ~ 0) dBm
Supply voltage monitor absolute error	DMI_VCC	-3	3	%	
Bias current monitor absolute error	DMI_Ibias	-10	10	%	
No-power monitor RX		-40		dBm	
Tx_disable power monitor		-40		dBm	

Table8-Control and Status I/O Timing Characteristics

PARAMETER	Symbol	Min	Max	Unit	Note
MgmtInitDuration	Max MgmtInit		2000	ms	Note1
ResetL Assert Time	t_reset_init	10		us	Note2
IntL Assert Time	ton_IntL		200	ms	Note3
IntL Deassert Time	toff_IntL		500	us	Note4
Rx LOS Assert Time	ton_los		100	ms	Note5
Rx LOS Assert Time (optional fast mode)	ton_losf		10	ms	Note6
Rx LOS Deassert Time	toff_los		100	ms	
Tx Fault Assert Time	ton_Txfault		200	ms	Note7
Flag Assert Time	ton_flag		200	ms	Note8
Mask Assert Time	ton_mask		100	ms	Note9
Mask Deassert Time	toff_mask		100	ms	Note10
High power up state			180	s	
Software TX disable assert time			100	ms	
Software TX disable de-assert time			10	s	

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State

[2] Minimum pulse time on the ResetL signal to initiate a module reset
[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol
[4] Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS,Tx Fault and other flag bits
[5] Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted
[6] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted
[7] Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted
[8] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted
[9] Time from mask bit set (value=1b) until associated IntL assertion is inhibited
[10] Time from mask bit cleared (value=0b) until associated IntL operation resumes

Table9-IIC 2-wire specification

PARAMETER	Symbol	Fast Mode (400 KHz)		Fast Mode Plus(1 MHz)		Unit	Conditions
		Min	Max	Min	Max		
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.5		µs	
Clock Pulse Width Hig	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.6		us	
STOP Hold Time	tHD.STO	0.6		0.26		us	
Aborted sequence - bus release	Deselect_Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the

Time1							setup time on the select lines before the start of a host initiated serial bus sequence.
ModSelL Hold Time1	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single Sequential Write	tWR		40		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50K			50K	cycles	Module Case Temperature = 70℃
Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.							

Reliability Test Definitions and Distributions

Table10-Reliability Test Definitions and Distributions

Group	Test	Reference	Condition	SS[1]	C[2]
Mechanical Integrity	Mechanical shock	MIL-STD-883E Method 2002.4	5 times/axis, 6 axes; 500G, 1.0ms	11	0
	Vibration	MIL-STD-883E Method 2007.3	20G, （20-2,000） Hz, 4 min/cycle，4 cycles/axial direction，3 axial direction	11	0
Endurance	Accelerated Aging	GR-468-Core 3..3.3.1	85℃(Ambient Temp.) Vcc=3.3V, 2,000hrs required	22	0
	High temperature Storage	GR-468-Core Issue 2, Section 3.3.2.1	85 °C (Ambient Temp.), 2000hrs	11	0
	Low temperature Storage	GR-468-Core Issue 2, Section 3.3.2.1	–40°C (Ambient Temp.), 72 hours	11	0
	Temperature Cycles	GR-468-Core Issue 2, Section 3.3.2.2 or MIL-STD-883C Method 1010.8	-40℃/85℃, 100 cycles (CO environment), 500 cycles (UNC environment)	11	0
	Damp Heat	GR-468-CORE 3.3.2.3	85℃/85%RH，500h	11	0

	Cyclic moisture resistance	MIL-STD-883E Method 1004.7	No preconditioning. Normal operating conditions. Ramp Time below zero to min storage temp should be rapid or with fast ramp time. Minimum of 20 cycles with 10 sub-cycles. Active Components and Modules. 20 cycles, w/ 5 sub-cycles.	11	0
ESD threshold	ESD Immunity	IEC 61000-4-2	In terms of 8Kv package contact ESD test and air discharge ESD 15KV test, it is allowed that bit-error occurring during the test, but the bit-error shall be able to recover automatically.	6	0
	ESD (HBM model)	GR-468-CORE、JESD22-A114-B	The modules should meet ESD threshold value requirement which defined in GR-468-CORE , as well as in MSA documents . for example, high speed interface, XFP XFI pin, Serdes should meet HBM 500v ESD requirement , the other interface should meet above 2KV HBM ESD level.	6	0

Notes：

[1] SS: Sample Size;

[2] C: Maximum number of failure allowed in the test.

Pin-out Definitions

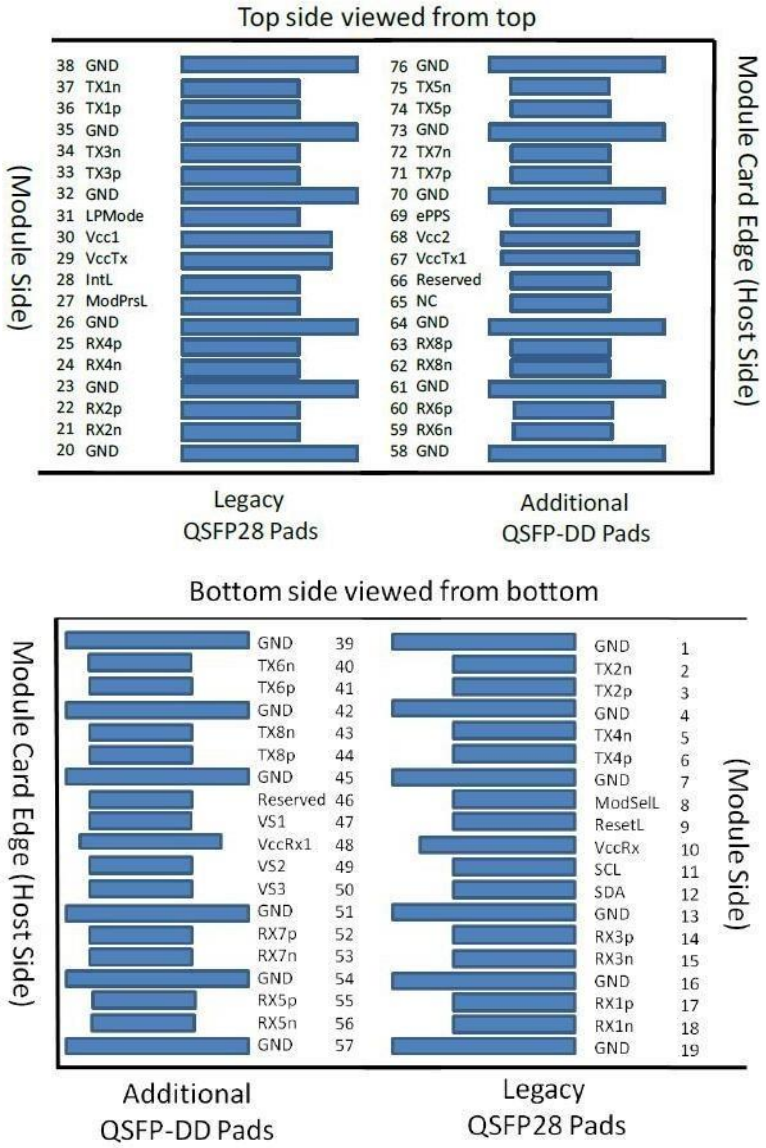

Figure 1 Module pad layout

Table11--Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Plug Sequence[4]	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	

6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	

60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input. Not used	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

[1] QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently.Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500 mA.

[3] All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

Block Diagram of Transceiver

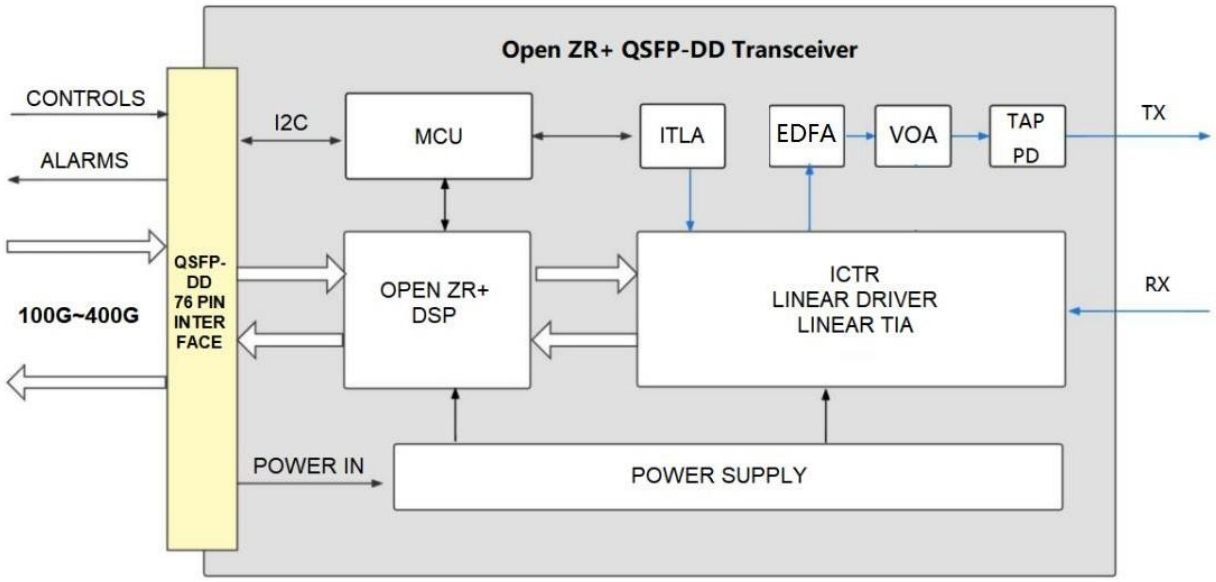

Figure 2 Block Diagram of Transceiver

Recommended Interface Circuit

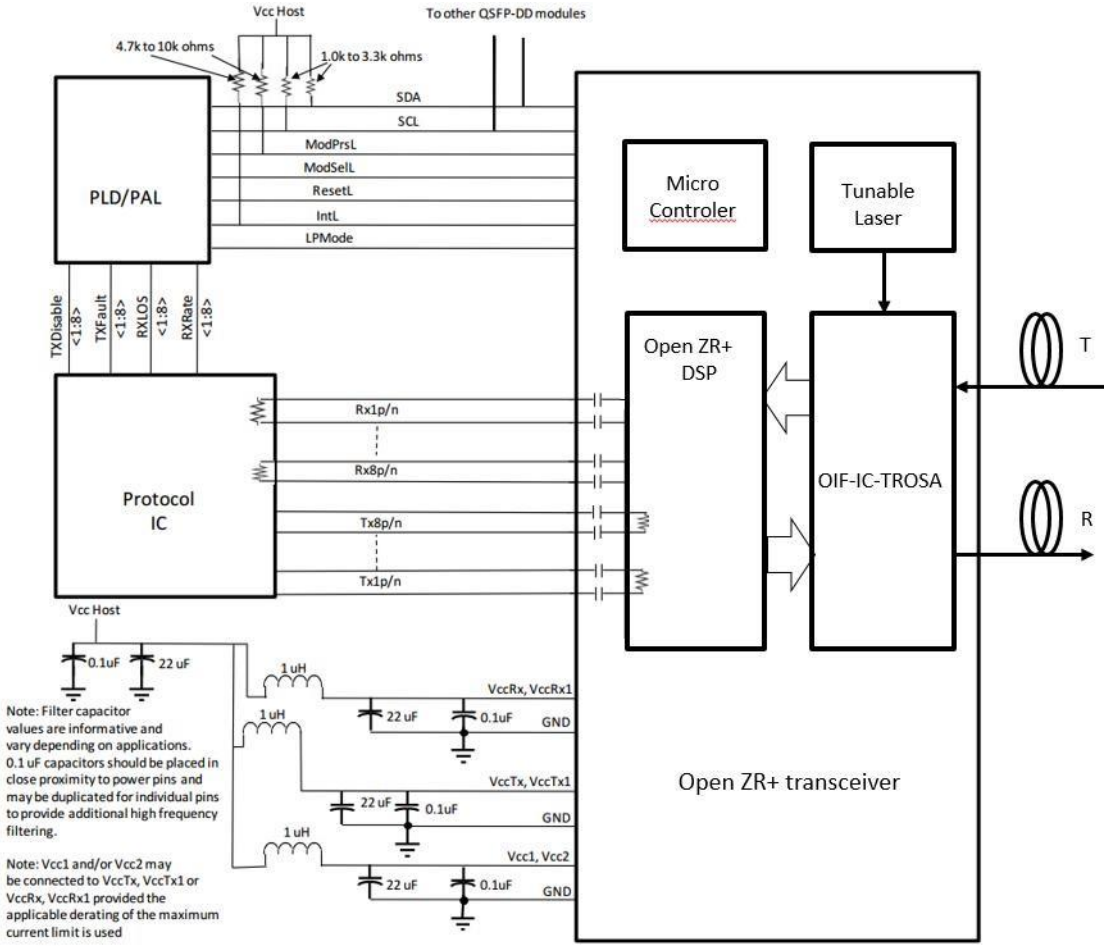

Figure 3 Recommended Interface Circuit

Dimensions

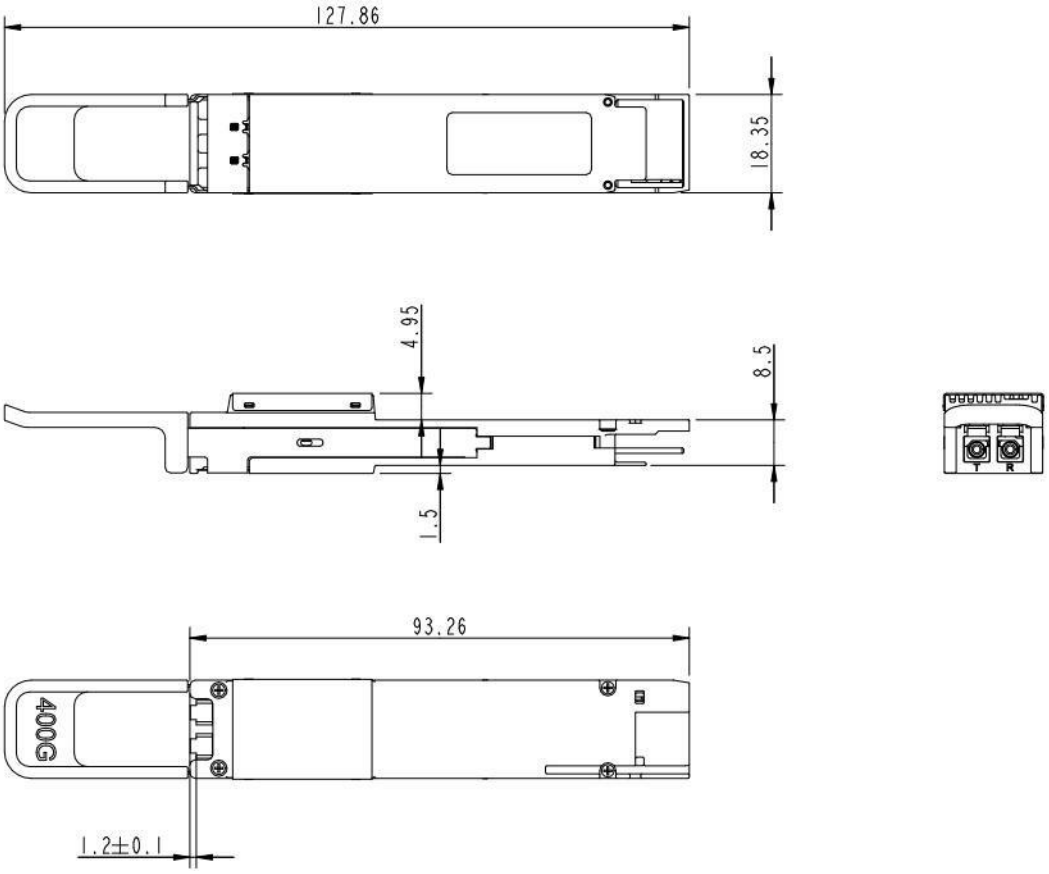

Figure 4 Dimensions

EEPROM Information

Table12-DDM Alarm & warning threshold

Parameters	Unit	threshold	Description
Temp low warning	℃	0	Min. case temperature
Temp high warning	℃	70	Max. case temperature
Voltage low warning	V	3.135	-5% Vcc target
Voltage high warning	V	3.465	+5% Vcc target
Tx power low warning	dBm	P_{set} - 2dBm	P_{set} is the configured output power
Tx power high warning	dBm	P_{set} + 2dBm	P_{set} is the configured output power
Rx power low warning	dBm	Configurable	Configurable, default -14dBm for 400ZR+
Rx power high warning	dBm	Configurable	Configurable, default 2dBm for 400ZR+
laser temp low warning	℃	-3	
laser temp high warning	℃	75	
Temp low alarm	℃	-10	
Temp high alarm	℃	80	

Voltage low alarm	V	3.05	
Voltage high alarm	V	3.5	
Tx power low alarm	dBm	P_{set} - 3dBm	P_{set} is the configured output power
Tx power high alarm	dBm	P_{set} + 3dBm	P_{set} is the configured output power
Rx power low alarm	dBm	Configurable	Configurable, default -16dBm for 400ZR+
Rx power high alarm	dBm	Configurable	Configurable, default 5dBm for 400ZR+
Optional laser temp low alarm	℃	-10	
Optional laser temp high alarm	℃	85	

Regulatory Compliance

Table13-Regulatory Compliance

Feature		Reference	Performance
Electrostatic discharge (ESD)		IEC/EN 61000-4-2	Compatible with standards
Electromagnetic Interference (EMI)		FCC Part 15 Class B EN 55022 Class B (CISPR 22A)	Compatible with standards
Laser Eye Safety		FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1，2	Class 1 laser product
Component Recognition		IEC/EN 60950 ， UL	Compatible with standards
ROHS		Directive 2011/65/EU & Directive (EU) 2015/863	Compatible with standards
EMC		EN61000-4-3	Compatible with standards
Safety regulation requirement	UL	UL60950-1	Compatible with standards
	TUV	IEC/EN60950-1，IEC/EN60825-1，IEC/EN60825-2；	Compatible with standards
	FDA	21 CFR 1040.10 & 1040.11	Compatible with standards

--Caution - use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Table14- Ordering Information

Part No.	Specification						
	Pack	Rate	Tx/RX	Pout	Top	Reach	Others
EN-QDD-DCO-ZR+ PRO	QSFP-DD	400G [1]	ICTR	-10~1dBm [2]	0 ~ 70℃	450km[1]	DDM/RoHS
EN-QDD-DCO-ZR+ PRO	QSFP-DD	400G	ICTR	4dBm[3]	0 ~ 70℃	80km[3]	DDM/RoHS

Notes:
[1] 400ZR+
[2] Not configure or configure to max power.
[3] 400G 80Km Gray mode

Notice:

E.C.I. Networks reserves the right to make changes to or discontinue any optical link product or service identified in this publication, without notice, to improve design and/or performance. Applications that are described herein for any of the optical link products are for illustrative purposes only.

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